WHAT IS CLAIMED IS;

1. A semiconductor device including a CMOS circuit having an NTFT and a PTFT, each of the NTFT and the PTFT including an active layer, an insulation film in contact with the active layer, and a wiring in contact with the insulation film, wherein

only the NTFT includes a side wall spacer on a side of the wiring,

the active layer of the NTFT includes a channel forming region and at least three kinds of impurity regions each containing an element belonging to the group 15 at a different concentration,

the impurity region in contact with the channel forming region among the three kinds of impurity regions overlaps by way of the insulation film with the side wall,

the active layer of the PTFT includes a channel forming region and two kinds of impurity regions each containing an element belonging to the group 13 at an identical concentration, and

an element used for crystallization of the active layer of the NTFT and the active layer of the PTFT is present at a concentration of 1×10^{17} to 1×10^{20} atoms/cm^3 in one of the impurity region most remote from the channel forming region of the NTFT and in one of the impurity region most remote from the channel forming region of the PTFT.

2. A semiconductor device having a CMOS circuit having an NTFT and a PTFT, each of the NTFT and the PTFT including an active layer, an insulation film in contact with the active layer and a wiring in contact with the insulation film, wherein

only the NTFT includes a side wall spacer on a side of the wiring,

the active layer of the NTFT includes a structure in which a channel forming region, a first impurity region, a second impurity region and a third impurity region are arranged in this order,

each of the first impurity region, the second impurity region and the third impurity region contains an element belonging to the group 15 at a different concentration,

the first impurity region overlaps by way of the insulation film with the side wall,

the active layer of the PTFT includes a structure in which a channel forming region, a fourth impurity region and a fifth impurity region are arranged in this order,

each of the fourth impurity region and the fifth impurity region contains an element belonging to the group 13 at an identical concentration and

an element used for the crystallization of the active layer is present at a concentration of 1×10^{17} to 1×10^{20} atoms/cm^3 in the third impurity region and the fifth impurity region.

3. A semiconductor device having a CMOS circuit having an NTFT and a PTFT each of the NTFT and the PTFT including an active layer, an insulation film in contact with the active layer and a wiring in contact with the insulation film, wherein

only the NTFT includes a side wall (spacer) on a side of the wiring,

the active layer of the NTFT includes a channel forming region and at least three kinds of impurity regions each containing an element belonging to the group 15 at a different concentration,

the concentration of the element belonging to the group 15 is higher as the distance from the channel forming region

is greater in at least three kinds of impurity regions,

the active layer of PTFT includes a channel forming region and two kinds of impurity regions containing an element belonging to the group 13 at an identical concentration, and

the active layer of PTFT includes a channel forming region and two kinds of impurity regions containing an element belonging to the group 13 at an identical concentration, and in which

an element used for the crystallization of the active layer is present at a concentration of 1×10^{17} to 1×10^{20} atoms/cm^3 in the impurity region most remote from the channel forming region of the NTFT and in the impurity region most remote from the channel forming region of the PTFT.

4. A semiconductor device including a CMOS circuit having an NTFT and a PTFT each of the NTFT and the PTFT including an active layer, an insulation film in contact with the active layer and a wiring in contact with the insulation film, wherein

only the NTFT includes a side wall spacer on a side of the wiring,

the active layer of the NTFT has a structure in which a channel forming region, a first impurity region, a second impurity region and a third impurity region are arranged in this order,

each of the first impurity region, the second impurity region and the third impurity region contains identical impurities at a different concentration,

the concentration of the impurities is higher in the order of the first impurity region, the second impurity region and the third impurity region,

the active layer of the PTFT has a structure in which a channel forming region, a fourth impurity region and a fifth impurity region are arranged in this order,

each of the fourth impurity region and the fifth impurity region contains an element belonging to the group 13 at an identical concentration, and

an element used for the crystallization of the active layer of the NTFT and the active layer of the PTFT is present at a concentration of 1 x 10^{17} to 1 x 10^{20} atoms/cm^3 in the third impurity region and the fifth impurity region.

5. A semiconductor device as claimed in any one of claims 1 to 4, wherein the active layer includes a single crystal semiconductor thin film.

6. A semiconductor device as claimed in any one of claims 1 to 4, wherein the element used for crystallization is at least one selected from Ni, Ge, Co, Fe, Pd, Sn, Pb, Pt, Cu, Au and Si.

7. A semiconductor device as claimed in any one of claims 1 to 4, wherein at least a portion of the wiring is covered with a silicon nitride film.

8. A semiconductor device as claimed in any one of claims 1 to 4, wherein the side wall includes silicon.

9. A semiconductor device as claimed in claim 1 or 3, wherein the element belonging to the group 15 is present in one of the impurity regions of the NTFT and in one of the impurity regions of the PTFT at a concentration identical with each other, the element used for crystallization being present in said one of the impurity regions of the NTFT and in said one of the impurity regions of the PTFT.

10. A semiconductor device as claimed in claim 2 or 4, wherein the element belonging to the group 15 is present in the third impurity region and in the fifth impurity region

at a concentration identical with each other.

11. A semiconductor device as claimed in claim 2 or 4, wherein the element belonging to the group 15 is present in the third impurity region and in the fifth impurity region at a concentration identical with each other, and the concentration of the element belonging to the group 15 is lower than the concentration of the element belonging to the group 13 present in the fifth impurity region.

12. A semiconductor device as claimed in claim 2 or 4, wherein the concentration of the impurity contained in the first impurity region is $1 \times 10^{15} - 1 \times 10^{17}$ atoms/cm^3, and the concentration of the impurity contained in the second impurity region is $1 \times 10^{16} - 1 \times 10^{19}$ atoms/cm^3.

13. A semiconductor device as claimed in any one of claims 1 to 4, wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

14. A semiconductor device as claimed in any one of claims 1 to 4, wherein the semiconductor device is one selected from a video camera, a digital camera, a projector, a goggle type display, a car navigation device, a personal computer and a portable information terminal.

15. A method of manufacturing a semiconductor device, comprising:

a first step of forming a semiconductor film containing crystals on a substrate having an insulation surface by using a catalyst element,

a second step of patterning the semiconductor film containing the crystals thereby forming a first active layer and a second active layer,

a third step of forming an insulation film on the first active layer and the second active layer,

a fourth step of forming wirings on the insulation film,

a fifth step of adding an element belonging to the group 15 to the first active layer and the second active layer using the wirings as a mask,

a sixth step of forming a side wall on a side of at least one of the wirings,

a seventh step of adding an element belonging to the group 15 to the first active layer and the second active layer using the wirings and the side wall as a mask,

an eighth step of forming a resist mask over the first active layer and adding an element belonging to the group 13 to the second active layer,

a ninth step of forming a resist mask on the first active layer and the second active layer and adding an element belonging to the group 15 to a portion of the first active layer and a portion of the second active layer,

a tenth step of forming a silicon nitride film, and

an eleventh step of gettering the catalyst element to a portion of the first active layer and to a portion of the second active layer by a heat treatment.

16. A method of manufacturing a semiconductor device as claimed in claim 15, wherein a concentration of the element belonging to the group 15 added in the ninth step is lower than a concentration of the element belonging to the group 13 added in the eighth step.

17. A semiconductor device as claimed in claim 15, wherein the side wall includes silicon.

18. A semiconductor device as claimed in claim 15, wherein the semiconductor film is a single crystal semiconductor thin film.

19. A semiconductor device as claimed in claim 15, wherein a first impurity region a second impurity region and

a third impurity region each containing an element belonging to the group 15, and a channel forming region are formed in the first active layer,

a fourth impurity region and a fifth impurity region each containing an element belonging to the group 13 at an identical concentration, and a channel forming region are formed in the second active layer, and

an element belonging to the group 15 is contained in the third impurity region and in the fifth impurity region at a concentration identical to each other.

20. A semiconductor device as claimed in claim 19, wherein a concentration of the element belonging to the group 15 is made higher in the order of the first impurity region, the second impurity region and the third impurity region.

21. A method of manufacturing a semiconductor device, comprising:

a first step of forming an active layer containing a catalyst element for promoting the crystallization on a substrate having an insulation surface,

a second step of forming a first insulation film on the active layer,

a third step of forming a wiring on the first insulation film,

a fourth step of adding an element belonging to the group 15 to the active layer using the wirings as a mask,

a fifth step of forming a side wall on a side of the wiring,

a sixth step of adding an element belonging to the group 15 to the active layer using the wiring and the side wall as a mask,

a seventh step of removing a portion of the first

insulation film thereby exposing a portion of the active layer formed in the sixth step,

an eighth step of adding an element belonging to the group 15 to the active layer exposed in the seventh step,

a ninth step of forming a second insulation film in contact with an upper portion of the wiring, and

a tenth step of applying a heat treatment for decreasing the concentration of the catalyst element in the active layer.

22. A method of manufacturing a semiconductor device, comprising:

a first step of forming a first active layer and a second active layer containing a catalyst element for promoting the crystallization on a substrate having an insulation surface,

a second step of forming a first insulation film on the first active layer and the second active layer,

a third step of forming wirings over the first active layer and the second active layer,

a fourth step of adding an element belonging to the group 15 to the first active layer and the second active layer using the wirings as a mask,

a fifth step of forming a side wall on a side of at least one of the wirings,

a sixth step of adding an element belonging to the group 15 to the first active layer and the second active layer using the wirings and the side wall as a mask,

a seventh step of selectively removing a portion of the first insulation film thereby exposing a portion of the first active layer and a portion of the second active layer formed in the sixth step,

an eighth step of adding an element belonging to the

group 15 to the first active layer and the second active layer exposed in the seventh step,

a ninth step of forming a second insulation film in adjacent with an upper portion of the wirings,

a tenth step of applying a heat treatment for decreasing the concentration of the catalyst element in the first active layer and the second active layer,

an eleventh step of selectively removing the second insulation film thereby exposing a portion of the second active layer formed in the tenth step,

a twelfth step of removing the second active layer exposed in the eleventh step,

a thirteenth step of selectively removing the insulation film thereby exposing a portion of the second active layer, and

a fourteenth step of adding an element belonging to the group 13 to the second active layer exposed in the thirteenth step.

23. A method of manufacturing a semiconductor device as claimed in claim 22, wherein at least three kinds of impurity regions each containing an element belonging to the group 15 at a different concentration, and a channel forming region are formed in the first active layer, and wherein only the channel forming region and the fourth impurity region are formed in the second active layer.

24. A method of manufacturing a semiconductor device as claimed in claim 22, wherein the channel forming region, the first impurity region, the second impurity region and the third impurity region are formed in the first active layer, and wherein only the channel forming region and the fourth impurity region are formed in the second active layer finally.

25. A method of manufacturing a semiconductor device as claimed in claim 24, wherein a concentration of the element belonging to the group 15 is made higher in the order of the first impurity region, the second impurity region and the third impurity region.

26. A method of manufacturing a semiconductor device as claimed in claim 21 or 22, wherein at least three kinds of impurity regions each containing an element belonging to the group 15 at a different concentration and a channel forming region are formed in the first active layer.

27. A method of manufacturing a semiconductor device as claimed in claims 24 or 25, wherein the side wall is formed above the first impurity region.

28. A method of manufacturing a semiconductor device as claimed in claim 24 or 25, wherein a concentration of the element belonging to the group 15 is made higher in the order of the first impurity region, the second impurity region and the third impurity region.

29. A method of manufacturing a semiconductor device as claimed in any one of claims 15 to 25, wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

30. A method of manufacturing a semiconductor device as claimed in any one of claims 15 to 25, wherein the semiconductor device is one selected from a video camera, a digital camera, a projector, a goggle type display, a car navigation device, a personal computer and a portable information terminal.